CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. an integrated circuit (IC) chip comprising:

the chip comprising a base substrate, a plurality of stacked levels of conductive metallurgy and low-k dielectric material fabricated over the substrate, the conductive metallurgy including active electrical lines, with the conductive metallurgy in different levels being connected by conductive metallurgy vias, and being capped by a top oxide cap covering the plurality of stacked levels;

a plurality of stacked via pillars positioned at a plurality of spaced locations in the chip, wherein the plurality of stacked via pillars extend completely from the base substrate of the chip to the top oxide cap of the chip, and at least a portion of the plurality of stacked via pillars are not electrically connected to any of the active electrical lines or vias, wherein the plurality of stacked via pillars support the structural stability of the chip design to accommodate deformations during any thermal and/or mechanical stresses.

2. The chip of claim 1, wherein the stacked via pillars are formed of the same conductive material as the conductive metallurgy vias in the chip.

3. The chip of claim 1, wherein the stacked via pillars are formed of a high modulus, low coefficient of thermal expansion material, such as SiO2 and SiN, which is different from the conductive material forming the conductive metallurgy vias in the chip.

4. The chip of claim 1, wherein at least some of the stacked via pillars are electrically connected to the active electrical lines or vias to provide an additional function of providing an electrical connection in the chip.

5. The chip of claim 1, wherein the stacked via pillars are arranged in a nested regular array, wherein the spacing between adjacent stacked via pillars is determined by the total amount of conductive metallurgy in an interconnection structure of the chip.

6. The chip of claim 1, wherein the spacing between adjacent stacked via pillars is determined by the total amount of conductive metallurgy in an interconnection structure of the chip, which is used to determine a horizontal parameter representing a fraction of the total amount of metallurgy fill to the total amount of material including dielectric material in the horizontal direction in the interconnection structure of the chip, and to determine a vertical parameter representing a fraction of the total amount of metallurgy fill to the total amount of material including dielectric material in the vertical direction in the interconnection structure of the chip.

7. The chip of claim 1, wherein the plurality of stacked via pillars extend in a straight linear line from the base substrate of the chip to the top oxide cap of the chip.

8. The chip of claim 1, wherein the plurality of stacked via pillars are positioned in a regular nested array on the chip, and the spacing between adjacent stacked via pillars is determined by the total amount of conductive metallurgy in an interconnection structure of the chip, which is used to determine a horizontal parameter representing a fraction of the total amount of metallurgy fill to the total amount of material including dielectric material in the horizontal direction in the interconnection structure of the chip, and to determine a vertical parameter representing a fraction of the total amount of metallurgy fill to the total amount of material including dielectric material in the vertical direction in the interconnection structure of the chip.

9. The chip of claim 1, wherein the active electrical lines and vias are wired around the plurality of stacked via pillars.

10. The chip of claim 1, wherein the chip is first designed and laid out in an interim design, and a fraction of total metallurgy to total material in the interim design of an interconnection structure of the chip is used to determine a minimum spacing between the plurality of stacked via pillars.

11. A method of designing an integrated circuit (IC) chip comprising:

designing the chip with a base substrate, a plurality of stacked layers of conductive metallurgy and low-k dielectric material fabricated over the substrate, with the conductive metallurgy including active electrical lines, and the conductive metallurgy in different layers being connected by conductive metallurgy vias, and being capped by a top oxide cap;

incorporating in the design of the chip a plurality of stacked via pillars positioned at spaced locations in the chip, wherein the plurality of stacked via pillars extend completely from the base substrate of the chip to the top oxide cap of the chip, and at least a portion of the plurality of stacked via pillars are not electrically connected to any of the active electrical lines or vias, wherein the plurality of stacked via pillars support the chip structure to accommodate radial deformations during any thermal and/or mechanical stresses.

12. The method of claim 11, including designing the stacked via pillars to be fabricated of the same conductive material as the conductive metallurgy vias in the chip.

13. The method of claim 11, including designing the stacked via pillars to be fabricated of a high modulus, low coefficient of thermal expansion material, such as SiO2 and SiN, which is different from the conductive material forming the conductive metallurgy vias in the chip.

14. The method of claim 11, including designing at least some of the stacked via pillars to electrically connect to the active electrical lines or vias to provide an additional function of providing an electrical connection in an interconnection structure of the chip.

15. The method of claim 11, including designing the spacing between adjacent stacked via pillars by determining the total amount of conductive metallurgy in an interconnection structure of the chip.

16. The method of claim 11, including designing the spacing between adjacent stacked via pillars by determining the total amount of conductive metallurgy in an interconnection structure of the chip and determining a horizontal parameter representing a fraction of the total amount of metallurgy fill to the total amount of material including dielectric material in the horizontal direction in the interconnection structure of the chip, and determining a vertical parameter representing a fraction of the total amount of metallurgy fill to the total amount of

material including dielectric material in the vertical direction in the interconnection structure of the chip.

17. The method of claim 11, including designing the plurality of stacked via pillars to be positioned in a regular nested array on the chip, and determining the spacing between adjacent stacked via pillars by the total amount of conductive metallurgy in an interconnection structure of the chip.

18. The chip of claim 11, including designing the plurality of stacked via pillars to be positioned in a regular nested array on the chip, and determining the spacing between adjacent stacked via pillars by the total amount of conductive metallurgy in an interconnection structure of the chip, determining a horizontal parameter representing a fraction of the total amount of metallurgy to the total amount of material including dielectric material in the horizontal direction in the interconnection structure of the chip, and determining a vertical parameter representing a fraction of the total amount of metallurgy to the total amount of material including dielectric material in the vertical direction in the interconnection structure of the chip.

19. The method of claim 11, including incorporating the design of the plurality of stacked via pillars in a chip template, and routing the active electrical lines and vias around the plurality of stacked via pillars.

20. The method of claim 11, including first designing and laying out the design of the chip in an interim design, and then determining the fraction of total metallurgy to total material in an interconnection structure of the interim design of the chip, and then using the determined fraction to determine a minimum spacing for the stacked via pillars.